## REMARKS

The present application is a Rule 60 continuation of parent application Serial No. 08/374,421, filed January 19, 1995, now U.S. Patent No. 5,657,206, issued August 12, 1997. This Amendment A is submitted in response to the Office Action mailed November 3, 1997.

Applicant is submitting a Terminal Disclaimer and Rule 3.73(b) Certificate, both of which are properly executed by applicant herein in order to overcome the obviousness-type double patenting rejection raised by the Examiner in view of applicant's now issued Patent No. 5,657,206. It is therefore requested that the Examiner withdraw his rejection of Claims 1-15 based upon the double patenting rejection.

Applicant has amended the title of the invention to be more clearly indicative of the invention to which the claims are directed, as required by the Examiner in the parent application.

The Examiner rejected Claims 11 and 15 as indefinite. Applicant has amended Claim 11 to recite that the chip is face-up on the substrate and Claim 15 to recite that the beveled edge walls are located at the outer edges of the chip and sloping toward the center of the chip, as described, for example, at page 14, lines 7+ of the specification. It is believed that Claims 11 and 15 are now in compliance with 35 USC § 112, second paragraph. In addition, applicant has made minor amendments to the pending claims to more clearly recite the functions of "depositing", "placing", and "applying" in lieu of the prior recitation of "disposing". Applicant has also amended several of the claims to recite "bond pads", rather than "inner bond pads".

The Examiner rejected Claims 1-15 under 35 USC § 103 as being unpatentable over Japanese reference 63-56925 ( the "Sai" reference). The Examiner cited the Sai reference in

initially characterizing Claims 1-15 as obvious. The Examiner pointed out that the Sai reference discloses the claimed invention except that Sai "uses solder instead of an electrically conductive adhesive to establish the electrical connection between external connection points of the chip and the terminals of the substrate". The Examiner stated that "the functional equivalency and interchange ability between solder and electrically conductive adhesive is well recognized in the art".

Applicant respectfully disagrees with the above statement and the Examiner is requested to cite authority for the above statement. It is respectfully submitted that it would not have been obvious to merely interchange electrically conductive epoxy as used by applicant herein with solder as used by Sai for several reasons.

Conductive epoxy is a totally different material and requires a totally different process when utilized for electrically connecting an integrated circuit chip to a PCB. The material requirement and method of die preparation for successful electrical connection using epoxy are different than those required for successful use of solder. More specifically, Claims 1-15 and new Claims 16-18 recite the incorporation of a metal layer for making an electrical contact with the bond pads, and where the metal layer forms external connection points such that the metal layer routes respective bond pads to corresponding external connection points, as now more clearly recited in Claims 1-18.

In contrast, Sai electrically connects the conductor electrodes 3A and 4A with solder layer 5 (solder layer 5A is used to keep mechanical adhesion between insulating films 7). There is no suggestion or teaching in Sai of a metal layer which is in electrical contact with the bond pads and which forms external connection points such that the metal layer routes respective bond



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pads to form corresponding external connection points, and where the conductive epoxy forms an electrical connection between the external connection points and the terminals of the substrate.

As described in the specification at page 10, lines 17+, the present invention provides the appropriate mechanical and material characteristics for connection to the epoxy. In addition to allowing the use of a different material for good bonding to the epoxy, the addition of the metal layer allows applicant to perform appropriate surface preparation steps to make the use of the epoxy practical. By depositing the epoxy directly on the original connection points present on the chip, as the examiner suggests can be inferred from the Sai reference, will not provide good electrical contact. Furthermore, the original contact locations on the chip are too close together to allow deposition of epoxy without neighboring epoxy contacts shorting. The metal layer recitation also serves to allow the locations for connection to be spread out over a wider area to avoid the problem of adjacent connection points shorting. It is therefore believed that the conduction and interface contact mechanism for epoxy is vastly different from solder and therefore surface conditioning and material composition requirements are entirely different for solder vs. conductive epoxy.

Further documentation of distinctions between conductive epoxy and solder are believed to be described in U.S. Patent Nos. 5,074,947; 5,195,371;5,237,130; and 5,611,140, copies of which are being submitted with applicant's Information Disclosure Statement (see, for example, the respective background descriptions of the above '947; '371; '130; and '140 patents).

The use of conductive epoxy by applicant also permits a lower curing temperature (e.g., curing the conductive epoxy at 120°C for 60 minutes in one preferred embodiment), as contrasted with Sai's use of solder, which is believed to require a temperature environment of



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approximately 225°C.

The use of conductive epoxy provides an electrical connection which is more flexible in its nature than solder. Conductive epoxy is more compliant than solder, which when after much higher thermal cycling, results in a more rigid, fixed and non-compliant bond than conductive epoxy.

Conductive epoxy is much more suitable to being reworked than would be the case of solder in a PCB-chip environment as called for in Claims 1-15 now pending herein. It is therefore believed that there is nothing in Sai to suggest or teach the electrically conductive epoxy recitation in applicant's package and corresponding method as called for in Claims 1-15 .

In addition, another aspect of applicant's invention further distinguishes over Sai in that a minimum bond line thickness is maintained between the chip and PCB by including a number of spheres such as glass spheres of a known size within the conductive epoxy so as to maintain a certain distance D between the chip and the PCB. There is nothing in Sai to suggest or teach this very desirable aspect, as now recited more clearly in Claims 16-18.

Regarding the Sai reference, there must be some reason, suggestion or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the claimed combination and that knowledge cannot come from applicant's invention itself. In re Oetiker, 24 USPQ2d 1443 (Fed. Cir. 1992).

It is submitted that not only does Sai fail to provide a clear suggestion of the claimed subject matter of the present invention, Sai does not provide even the slightest suggestion in the art of applicant's claimed conductive epoxy recitation. Kimberly-Clark Corp. v Johnson & Johnson, 223 USPQ 603 (Fed. Cir. 1984).



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In view of the foregoing, it is believed that Claims 1-18 pending herein are now in condition for allowance.

Respectfully submitted,

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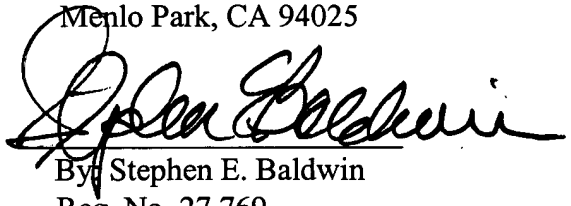

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